Amendments to the Claims:

The following listing of claims will replace all prior versions of claims in the application, wherein additions are shown in underlined text and deletions are shown in strike-out text:

1.–30. (Canceled)

31. (Canceled)

32. (Currently Amended) A silicon processing method, comprising: ~~The silicon processing method of claim 31, further comprising:~~

(a) providing a silicon substrate comprising a top side, a bottom side, and a bulk region;

(b) forming an ohmic contact anode on the bottom side of the silicon substrate;

(c) forming a masking layer comprising a bilayer of silicon dioxide and polycrystalline silicon on the top side of the silicon substrate and then patterning the masking layer, thereby exposing a portion of the top side of the silicon substrate;

(d) forming a sealed microchannel by performing an electrochemical process, the electrochemical process comprising:

(i) anodizing with a first current density below the critical value for electropolishing, thereby forming a porous silicon capping layer in the exposed portion of the top side of the silicon substrate, and then

(ii) anodizing with a second current density above the critical value for electropolishing, thereby dissolving a portion of the silicon substrate and forming a microchannel below the porous silicon capping layer;

(e) after step (d), depositing a thin dielectric isolation layer on the top side of the silicon substrate;

(f) performing a first deposition process, comprising:

(i) depositing a first polysilicon layer on the thin dielectric isolation layer;

(ii) patterning the first polysilicon layer to form a heater located above the porous silicon capping layer and a first branch of thermocouples located partially above the porous silicon capping layer and partially above the bulk region of the silicon substrate; and,

(iii) doping the first polysilicon layer with a p-type dopant;

(g) performing a second deposition process, comprising:

(i) depositing an aluminum layer on the thin dielectric isolation layer; and,

(ii) patterning the aluminum layer to form a second branch of thermocouples, interconnections, and metal pads, wherein the interconnections and the

metal pads are in separate electrical contact with the heater, the first branch of thermocouples, and the second branch of thermocouples;

(h) depositing a passivation layer above the top side of the semiconductor substrate, wherein the passivation layer is selected from the group consisting of an insulating layer, a silicon oxide layer, a silicon nitride layer, and a polyimide layer.

33. (Previously Presented) An infrared radiation detector comprising a silicon thermal sensor produced by the silicon processing method of claim 32.

34. (Previously Presented) A thermoelectric power generator comprising a silicon thermal device produced by the silicon processing method of claim 32.

35. (Currently Amended) A silicon processing method, comprising: ~~The silicon processing method of claim 31, further comprising:~~

(a) providing a silicon substrate comprising a top side, a bottom side, and a bulk region;

(b) forming an ohmic contact anode on the bottom side of the silicon substrate;

(c) forming a masking layer comprising a bilayer of silicon dioxide and polycrystalline silicon on the top side of the silicon substrate and then patterning the masking layer, thereby exposing a portion of the top side of the silicon substrate;

(d) forming a sealed microchannel by performing an electrochemical process, the electrochemical process comprising:

(i) anodizing with a first current density below the critical value for electropolishing, thereby forming a porous silicon capping layer in the exposed portion of the top side of the silicon substrate, and then

(ii) anodizing with a second current density above the critical value for electropolishing, thereby dissolving a portion of the silicon substrate and forming a microchannel below the porous silicon capping layer;

(e) after step (d), depositing a thin dielectric isolation layer on the top side of the silicon substrate;

(f) performing a first deposition process, comprising:

(i) depositing a first polysilicon layer on the thin dielectric isolation layer, a portion of which first polysilicon layer is located above the porous silicon capping layer;

(ii) patterning the first polysilicon layer to form a heater located above the porous silicon capping layer and a first branch of thermocouples; and,

(iii) doping the first polysilicon layer with a p-type dopant;

(g) performing a second deposition process, comprising:

(i) depositing an n-doped polycrystalline silicon layer on the thin dielectric isolation layer,

(ii) patterning the n-doped polycrystalline silicon layer to form a second branch of thermocouples;

(h) performing a third deposition process, comprising:

(i) depositing an aluminum layer on the thin dielectric isolation layer; and,

(ii) patterning the aluminum layer to form interconnections and metal pads, wherein the interconnections and the metal pads are in separate electrical contact with the heater, the first branch of thermocouples, and the second branch of thermocouples; and,

(i) depositing a passivation layer above the top side of the semiconductor substrate, wherein the passivation layer is selected from the group consisting of an insulating layer, a silicon oxide layer, a silicon nitride layer, and a polyimide layer.

36. (Previously Presented) An infrared radiation detector comprising a silicon thermal sensor produced by the silicon processing method of claim 35.

37. (Previously Presented) A thermoelectric power generator comprising a silicon thermal device produced by the silicon processing method of claim 35.

38. (Currently Amended) A silicon processing method, comprising: ~~The silicon processing method of claim 31, further comprising:~~

(a) providing a silicon substrate comprising a top side, a bottom side, and a bulk region;

(b) forming an ohmic contact anode on the bottom side of the silicon substrate;

(c) forming a masking layer comprising a bilayer of silicon dioxide and polycrystalline silicon on the top side of the silicon substrate and then patterning the masking layer, thereby exposing a portion of the top side of the silicon substrate;

(d) forming a sealed microchannel by performing an electrochemical process, the electrochemical process comprising:

(i) anodizing with a first current density below the critical value for electropolishing, thereby forming a porous silicon capping layer in the exposed portion of the top side of the silicon substrate, and then

(ii) anodizing with a second current density above the critical value for electropolishing, thereby dissolving a portion of the silicon substrate and forming a microchannel below the porous silicon capping layer;

(e) after step (d), depositing a thin dielectric isolation layer on the top side of the silicon substrate;

(f) performing a first deposition process, comprising:

(i) depositing a first polysilicon layer on the thin dielectric isolation layer; and,

(ii) patterning the first polysilicon layer to form a central heater, a left resistor, and a right resistor;

(g) performing a second deposition process, comprising:

(i) depositing an aluminum layer on the thin dielectric isolation layer; and,

(ii) patterning the aluminum layer to form interconnections and metal pads in separate electrical contact with the central heater, the left resistor, and the right resistor;

(h) selectively etching a left portion of the thin dielectric isolation layer and a left portion of the top side of the silicon substrate to form an inlet to the ~~microfluidic channel~~ microchannel;

(i) selectively etching a right portion of the thin dielectric isolation layer and a right portion of the top side of the silicon substrate to form an outlet to the ~~microfluidic channel~~ microchannel; and,

(j) depositing and patterning a passivation layer above the semiconductor substrate, wherein the passivation layer is selected from the group consisting of a silicon oxide layer, a silicon nitride layer, and a polyimide layer.

39. (Previously Presented) A thermal flow sensor comprising:

(a) a silicon substrate comprising a bulk region, a top side, a bottom side, a microchannel disposed therein, and a porous silicon capping layer aligned with the top side and locally formed above the microchannel;

(b) an ohmic contact anode on the bottom side of the silicon substrate;

(c) a thin dielectric isolation layer on the top side of the silicon substrate;

(d) a heater on the thin dielectric isolation layer above the porous silicon capping layer, the heater comprising a p-doped patterned polysilicon layer;

(e) a first thermocouple on the thin dielectric isolation layer, a portion of which is above the porous silicon capping layer and a portion of which is above the bulk region, the first thermocouple comprising a p-doped patterned polysilicon layer;

(f) a second thermocouple on the thin dielectric isolation layer, a portion of which is above the porous silicon capping layer and a portion of which is above the bulk region, the second thermocouple comprising a patterned aluminum layer or an n-doped patterned polysilicon layer;

(g) aluminum interconnects and aluminum pads on the thin dielectric isolation layer above the bulk region, wherein the aluminum interconnects and the aluminum pads are in separate electrical contact with the heater, the first thermocouple, and the second thermocouple; and,

(h) a passivation layer above the top side of the semiconductor substrate,

wherein the passivation layer is selected from the group consisting of a silicon oxide layer, a silicon nitride layer, and a polyimide layer

40. (Currently Amended) A thermal microfluidic sensor comprising:

(a) a silicon substrate comprising a bulk region, a top side, a bottom side, a microchannel disposed therein, and a porous silicon capping layer aligned with the top side and locally formed above the microchannel;

(b) a thin dielectric isolation layer on the top side of the silicon substrate;

(c) a central polysilicon heater, a left polysilicon resistor, and a right polysilicon resistor on the thin dielectric isolation layer and above the porous silicon capping layer;

(d) aluminum interconnections and aluminum metal pads on the thin dielectric isolation layer, above the bulk region, and in separate electrical contact with the central polysilicon heater, the left polysilicon resistor, and the polysilicon right resistor;

(e) an inlet region to the microchannel through a left portion of the thin dielectric isolation layer and a left portion of the silicon substrate;

(f) an outlet region to the microchannel through a right portion of the thin dielectric isolation layer and a right portion of the silicon substrate; and,

(g) a passivation layer above the top side of the semiconductor substrate, wherein the passivation layer is selected from the group consisting of a silicon oxide layer, a silicon nitride layer, ~~or~~ and a polyimide layer.